IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Martin C. Roberts et al.	)	Examiner: Neal Berezsny
	)	
Serial No.: 09/745,780	)	Group Art Unit: 2823
	)	
Filed: December 21, 2000	)	Docket: 303.451US6
	)	
For: METHOD FOR FORMING AN INTEGRATED CIRCUIT INTERCONNECT USING A DUAL POLY PROCESS	)	

APPELLANTS' BRIEF ON APPEAL

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on April 18, 2005, from the Rejection of claims 38-45, 47-52, 54-59, 62-65 and 68-79 of the above-identified application, as set forth in the Final Office Action mailed December 16, 2004.

This Appeal Brief is accompanied by an authorization to charge the requisite fee set forth in 37 C.F.R. § 117(f) and any extension of time fee to Appellants' deposit account 19-0743. Applicants respectfully request reversal of the Examiner's rejection of pending claims

APPELLANTS' BRIEF ON APPEAL

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, Micron Technology, Inc., a Delaware corporation doing business at 8000 South Federal Way, P.O. Box 6, Boise, Idaho 83707-0006.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to the Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

Claims 38-45, 47-65 and 68-79 are pending and the subject of the present appeal. No other claims remain in the application.

All of the claims are also subject to an obviousness double patenting rejection which Appellants do not dispute. Appellants filed a Terminal Disclaimer July 1, 2004 which was apparently not considered since the obviousness double patenting rejection was still maintained. Once claims are allowed a new Terminal Disclaimer will be filed if for some reason the previous Terminal Disclaimer was insufficient for some reason unknown to Appellants.

4. STATUS OF AMENDMENTS

This application was originally filed on December 21, 2000, with claims 34-52 pending after entry of the Preliminary Amendment filed with the application which is a continuation of U.S. Serial Number 08/390,714 filed February 17, 1995 which remains pending.

Preliminary Amendment and Response to Restriction Requirement Office filed August 23, 2001.

Amendment and Response to Office Action filed February 22, 2002

Amendment and Response to Final Office Action filed September 5, 2002 with RCE.

Amendment and Response to first Office Action after RCE filed September 27, 2002.

Final Office Action after RCE was mailed April 10, 2003.

A Notice of Appeal was filed on July 10, 2003.

An Appeal Brief was filed October 10, 2003.

A new Office Action was issued April 12, 2004 rejecting all claims on the Tang patent.

Amendment and Response to Office Action of April 12, 2004 was filed August 6, 2004

Amendment and Response to Final Office Action was filed February 16, 2005

Advisory Action was issued March 8, 2005

This Appeal was filed April 18, 2005.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to a an intermediate structure for the manufacture of a semiconductor interconnect having a via formed in a first polysilicon layer to expose a buried contact region on a substrate and a second polysilicon layer formed in the via to form an electrical interconnect.

6. ISSUES PRESENTED FOR REVIEW

Were claims 38-45, 47-65 and 68-79 properly rejected under 35 U.S.C. § 102?

7. ARGUMENT

A. The Applicable Law

A court must consider not only the similarities, but also the "critical differences between the claimed invention and the prior art." *In re Bond*, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991).

It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).

A single prior art reference anticipates a patent claim if it expressly or inherently describes each and every limitation set forth in a patent claim. *Verdegaal Bros., Inc. v. Union Oil Co.,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Anticipation requires that missing descriptive material be "necessarily present" in a reference rather than "merely probably or possibly present in the prior art." *Trintec Industries v. Top-USA Corporation,* 63 USPQ2d 1597, 1599 (Fed. Cir. 2002), citing *In re Robertson,* 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) which, in turn, cited *Continental Can Co. USA, Inc. v Monsanto Co.,* 948 F.2d 1264, 1268, 20USPQ2d 1746, 1749 (Fed. Cir. 1991).

B. The Office Action has not shown where every element of the claims is alleged to be found in Tang et al

All of the pending claims (38–45, 47–65 and 68–79) were rejected under 35 USC § 102(e) as being anticipated by Appellants' Assignee's (Micron Technology, Inc.'s) U.S. Patent 5,506,172 which was issued April 9, 1996 to Sanh Tang, who is one of the two named co-inventors of the

present application.

Appellant has not admitted that the cited Tang patent is prior art, and reserved the right to swear behind it at a later date. Nevertheless, Appellant respectfully submits that the pending claims are distinguishable over what may be shown in Tang for the reasons argued.

At issue here is a simple factual issue of what is shown in the Tang patent relied upon by the Final Office Action.

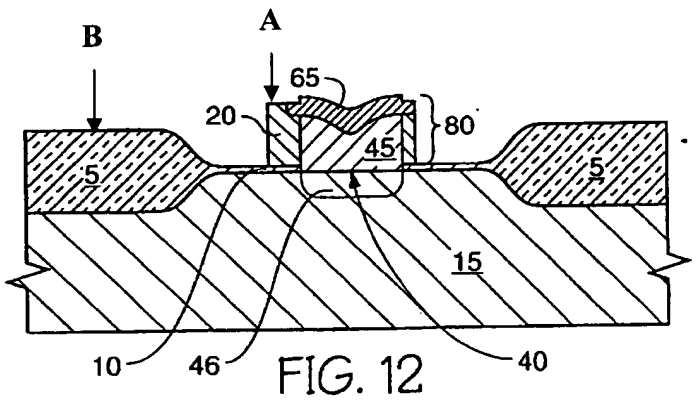

FIG. 12

The above Figure 12 is from Appellant's application. The only element of Appellant's claim 38 which is at issue here is:

> "a first polycrystalline silicon layer 20 overlying the oxide region 5 but not the first substrate region 40 and having a thickness selected such that a lowest upper surface **A** of the first polycrystalline silicon layer 20 is higher than a highest upper surface **B** of the oxide region[1]"

For the purposes of comparison, Appellant has reproduced below Figure 9 of the cited Tang patent[2]. Appellant has also reproduced Figure 6 of Tang which makes it clear that oxide layer 46 is a part of oxide layer 44. Finally, Appellant has added reference characters **C** and **D** to Figure 9 of Tang to designate where in Tang the surfaces **A** and **B** are located in Tang.

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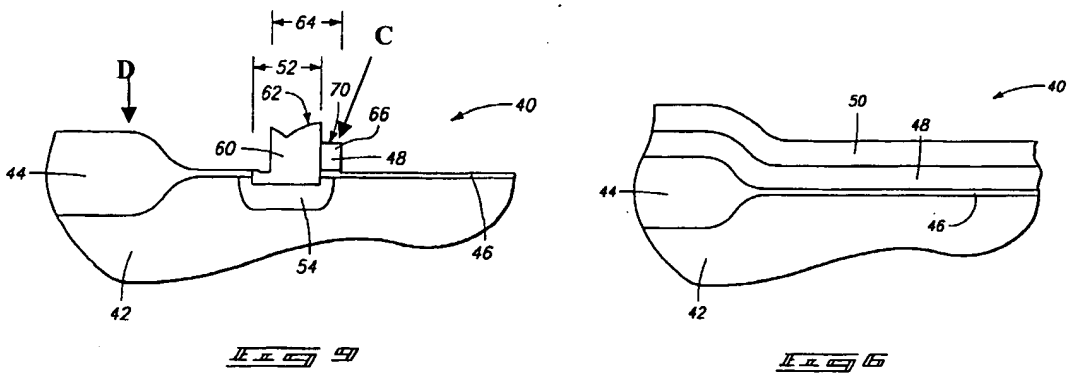
1 Appellant has added numerical reference characters corresponding to Appellant's patent specification showing respective claim elements in an embodiment of the invention claimed. Appellant has added alphabetic reference characters A and B to illustrate the surfaces called out in the claim.



In contrast to what claim 38 requires, Tang shows a structure where the first poly layer 48 has its lowest upper surface **C** either *lower than* or *about equal to* the highest upper surface **D** of oxide region 44. Furthermore, Tang's specification does not ascribe any particular importance to the relationship between the height of the lowest upper surface of the first polycrystalline layer 48 and the height of the highest upper surface of oxide layer 44 as Applicants' patent specification does[3]. Tang simply does not anticipate the height relationship that is specifically claimed in claim 38 and the other pending independent claims.

The Examiner responded to Appellants position that the height feature was not shown in Tang by contending that Tang oxide layer 46 was a different oxide layer than oxide 44 and that the claimed relationship was shown in Tang if just oxide 46 was considered in the comparison, ignoring the remainder of the layer which is designated with reference character 44 . Reference to Figure 6 of Tang reproduced above shows that layers 44 and 46 are parts of a single layer of oxide. In Tang the polysilicon layer does not have its thickness selected so that its lowest upper surface C is higher than a highest upper surface D of oxide layer 44, 46. Tang does not anticipate the quoted portion of claim 38.

In view of the clear distinction between what is claimed in the pending claims and what is shown in the cited Tang patent, the rejection fails to make a *prima facie* case of anticipation and

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2 The Examiner used the same figure in the Final Office Action.

3 See page 4, last line through page 5, lines 1–2.

should be withdrawn.

Dependent claims

The rejection of each of the dependent claims is unsustainable for the same reasons as explained for the parent independent claims.

C. Conclusion

The rejection which is the subject of this appeal is defective since it has not shown anticipation of any of the pending claims by the cited Tang patent. Reconsideration and withdrawal of the rejection and allowance of all of the pending claims is respectfully requested.

8. SUMMARY

For the foregoing reasons, the Appellant respectfully submits that the rejection of claims 38-45, 47-65 and 68-79 under 35 U.S.C. § 102(e) was erroneous. Reversal of those rejections is respectfully requested, as well as the allowance of all the claims.

Please charge Deposit Account 19-0743 to cover the fee required to file the Brief..

Respectfully submitted,

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Date

By _____
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Reg. No. 25,179

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450. 20231, on this 18th day of August, 2005.

Tina M. Kohl

_____
Signature

APPENDIX

The Claims on Appeal

38. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region; and

a second polycrystalline silicon layer overlying the first polycrystalline silicon layer and the first substrate region.

39. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region.

40. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide] region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region, the upper surface of the second polycrystalline silicon layer being substantially planar and aligned with the upper surface of the first polycrystalline silicon layer adjacent an interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer such that the interface has no horizontal component.

41. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

a field oxide region overlying at least a portion of the second substrate region;

a gate oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the field oxide and gate oxide regions but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide regions;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

42. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region and having the upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask of material resistant to polycrystalline silicon etching overlying the polycrystalline silicon plug and an adjacent portion of the first polycrystalline layer surrounding the polycrystalline silicon plug thereby defining an electrical interconnect.

43. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region and having an upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask overlying the polycrystalline silicon plug to define an electrical interconnect.

44. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the [field oxide and gate] oxide [regions] region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

45. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon plug overlying the first substrate region; and

a polycrystalline silicon layer overlying a portion of the oxide region adjacent the polycrystalline silicon plug, but not the first substrate region, the polycrystalline silicon layer having a thickness selected such that a lowest upper surface of the polycrystalline silicon layer is higher than a highest upper surface of the oxide region, the polycrystalline silicon layer also having an upper surface thereof in the region adjacent the polycrystalline silicon plug aligned with an upper surface of the polycrystalline silicon plug such that the vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component.

46. (Previously Canceled)

47. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying a portion of the oxide region adjacent the first substrate region, but not the first substrate region, and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

48. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium layer overlying the etch stop layer and the polycrystalline silicon plug layer.

49. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug;

a titanium layer overlying the etch stop layer; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

50. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first

polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

51. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a buried contact region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

52. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer partially overlying the oxide region adjacent the first substrate region but not overlying the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer

and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

53. (Previously Presented) The intermediate of claim 38 wherein the first substrate region includes a buried contact region.

54. (Previously Presented)The intermediate of claim 38 wherein a portion of the second polycrystalline layer overlying the first polycrystalline layer is removed to expose the first polycrystalline layer and eliminate a horizontal interface between the first and second polycrystalline silicon layers.

55. (Previously Presented) The intermediate of claim 39 wherein a portion of the second polycrystalline silicon layer overlying the first polycrystalline layer is removed so that a total height of the first polycrystalline silicon layer plus a height of the etch stop layer defines a maximum height of the second polycrystalline silicon layer after removal of the portion of the second polycrystalline silicon layer.

56. (Previously Presented) The intermediate of claim 40 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

57. (Previously Presented) The intermediate of claim 56 wherein the first and second polycrystalline silicon layers are doped with arsenic.

58. (Previously Presented) The intermediate of claim 41 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

59. (Previously Presented) The intermediate of claim 58 wherein the first and second polycrystalline silicon layers are doped with arsenic.

60. (Previously Presented) The intermediate of claim 42 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.

61. (Previously Presented) The intermediate of claim 43 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.

62. (Previously Presented) The intermediate of claim 44 wherein a photoresist mask is applied over a portion of the first etch stop layer and the second polycrystalline silicon layer.

63. (Previously Presented) The intermediate of claim 62 wherein a titanium layer is deposited to overlie the etch stop layer and the second polycrystalline silicon layer.

64. (Previously Presented) The intermediate of claim 45 wherein the polycrystalline plug and the polycrystalline silicon layer are doped to increase their conductivity.

65. (Previously Presented) The intermediate of claim 64 wherein the polycrystalline plug and the polycrystalline silicon layer are doped with arsenic.

66. - 67. (Canceled)

68. (Previously Presented) The intermediate of claim 47 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

69. (Previously Presented) The intermediate of claim 68 wherein the first and second polycrystalline silicon layers are doped with arsenic.

70. (Previously Presented) The intermediate of claim 48 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

71. (Previously Presented) The intermediate of claim 70 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

72. (Previously Presented) The intermediate of claim 49 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

73. (Previously Presented) The intermediate of claim 72 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

74. (Previously Presented) The intermediate of claim 50 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

75. (Previously Presented) The intermediate of claim 74 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

76. (Previously Presented) The intermediate of claim 51 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

77. (Previously Presented) The intermediate of claim 76 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

78. (Previously Presented) The intermediate of claim 52 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

79. (Previously Presented) The intermediate of claim 78 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

APPENDIX II

Cited Statutes, Rules, and Case law

I. Statutes and Rules

- 35 U.S.C. § 103(a)

II Case law

- *In re Bond*, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).
- *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991).
- *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)
- *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)
- *Trintec Industries v. Top-USA Corporation,* 63 USPQ2d 1597, 1599 (Fed. Cir. 2002)